AMENDMENTS TO THE SPECIFICATION

Please replace paragraph 25 with the following amended paragraph:

(25) Figure 6 depicts one embodiment of delta-sigma modulator 506 that includes an internal filter 602 used for integration and decimation of an input signal. Points “A” and points “B” represent the same data points as in Figure 5. The input data to delta-sigma modulator 600 is a discrete input signal sampled at $128*f_S$. Although the input signal is sampled at $128*f_S$, delta-sigma modulator 600 operates at $64*f_S$, one-half the frequency of the input signal. Thus, the input and output of delta-sigma modulator 600 effectively ~~operation~~ operate at two different frequencies.

Please replace paragraph 26 with the following amended paragraph:

(26) The internal filter 602 performs integration and 2-to-1 decimation by using the first two integration stages 604 and 606 to process successive pairs of input data samples, x(n) and x(n-1/2) and using a half-delay stage 608 with a z-domain transfer function of $z^{-1/2}$. Additional integration stages, such as integration stage 620 can be added as desired to alter the frequency response of delta-sigma modulator 600. The internal filter 602 achieves a high quality low-pass-filter frequency response by adjusting the gain of samples x(n) and x(n-1/2). Integration stages 604 and 606 can be implemented with a z-domain frequency response of z^{-1}, a feedback loop, and an input data summing operation. The input data to integration stage 604 is:

$$[[x(n-1/2)*g_{1,1} + x(n)\ g_{2,1} - c0*q.]]$$

$$\underline{x(n-1/2)*g_{1,1} + x(n)\ g_{2,1} - c1*q.}$$

The input data to integration stage 606 is:

$$[[I_1 + x(n-1/2)*g_{1,2} + x(n)\ g_{2,2} + c1*q.]]$$

$$\underline{I_1 + x(n-1/2)*g_{1,2} + x(n)\ g_{2,2} + c2*q.}$$

"$g_{1,1}$", "$g_{1,2}$", "$g_{2,1}$", and "$g_{2,2}$" represent respective gain stages 610, 612, 614, and 616. "I_1" represents the output data of integration stage 604. The output data of quantizer 618 provides negative feedback to each integration stage of delta-sigma modulator 600 adjusted by respective factors c1, c2, c3, and so on. In one embodiment, c0 is 0.5, and the remaining "c" factors are a matter of design choice. "Delta-Sigma Data Converters Theory, Design, and Simulation" by Norsworthy, et al., published by IEEE Press, 1997 includes information for determining the c1, c2, c3, and so on.

Please replace paragraph 27 with the following amended paragraph:

(27) The gains to the ~~fist~~ first integration stage 604, i.e. $g_{1,1}$ and $g_{2,1}$, and the gains to the second integration stage 606, i.e. $g_{1,2}$ and $g_{2,2}$, are independent linear combinations. In other words, $\frac{g_{2,2}}{g_{1,2}} \neq \frac{g_{2,1}}{g_{1,1}}$. Thus, ~~integrations~~ integration stages 604 and 606 receive a different mix of input signal pairs x(n) and x(n-1/2).

Please replace paragraph 29 with the following amended paragraph:

(29) Table 1 contains the empirically determined values of gains "g" ~~and quantizer output adjustment factors "c"~~ to achieve the frequency responses depicted in Figures 7, 8, 9, and 10. ~~Quantizer output adjustment factors~~

Figures	**$g_{1,1}$**	**$g_{2,1}$**	**$g_{2,2}$**	**$g_{1,2}$**
7 and 8	0.5	0.5	0	0.25
9 and 10	0.5	0.5	0.125	0.375

TABLE 1

The delta-sigma modulator 600 using the gains "g" Table 1 associated with Figures 7 and 8 ~~achieve~~ achieves a frequency response improvement of over 50 dB compared with the conventional frequency response depicted in Figures 3 and 4. The delta-sigma modulator 600 using the gains “g” ~~and factors “e”~~ in Table 1 associated with Figures 9 and 10 ~~achieve~~ achieves a frequency response improvement of over 65 dB compared with the conventional frequency response depicted in Figures 3 and 4.